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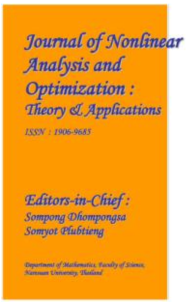

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Sompong Dhompongsa
Somyot Plubtieng
Department of Mathematics, Faculty of Science, Naresuan University, Thailand

DESIGN AND ANALYSIS OF A FIVE-LEVEL ONE-CAPACITOR BOOST MULTILEVEL INVERTER FOR GRID-CONNECTED PV SYSTEMS

[1]Dr.D.Srinivas,[2]V.Rajesh,[3]R.Divya,[4]Vemavarapu Rambabu
[1]Professor,[2]Associate Professor,[3]Assistant Professor,[4]Student
Department of EEE
G V R & S College of Engineering & Technology,Guntur,AP

ABSTRACT:

Low power Renewable Energy Generation Systems are one of the major uses for power electronic converters (REGS). This study proposes a new application for single phase grid connected multilevel inverter with one capacitor boost in REGS. Multilevel inverter systems are a good option for applications requiring medium to high power. This paper introduces a novel five-level (2Vdc, Vdc, 0, −Vdc, −2Vdc) boost multilevel inverter that is based on a single capacitor. The suggested formation's single-phase variant consists of one capacitor, eight switches, and a single dc source. The inverter uses the charge-pump theory, in which the capacitor charges in parallel and discharges in series connections to provide a greater output voltage, to give boosting ability. The level-shift pulse width modulation technique, in which the reference signal is compared with four carriers, is used to drive the switches and produce the necessary pulse pattern because the suggested setup calls for easy control chores. The created inverter has a few unique properties, including the ability to boost and the use of a single DC source and capacitor, as well as its compact size and straightforward control requirements. The system is simulated using MATLAB. The purpose of the simulation is to validate the functionality of the five-level configuration grid-connected solar system that has been built.

I.INTRODUCTION

In renewable energy systems, dc to ac conversion is typically required to generate the ac output with certain amplitude, frequency and small harmonic profile. Pulse width modulation (PWM) inverters with two-level or multilevel configurations are the mainstream ac/dc power electronic interfaces. They enable controlled amplitude, frequency and harmonics of the output voltage. Multilevel inverter configurations generate the ac output with reduced harmonic components. Hence, multilevel inverter topologies were covered extensively in the literature due to their merits such as small filter size and improved output waveform [1– 9]. In a multilevel inverter, multiple dc levels are used to synthesise a staircase waveform utilising power semiconductors. In comparison with two-level conventional inverters, multilevel inverters have improved harmonic profile and reduced semiconductor voltage stresses [10]. The power quality of multilevel inverter improves with the increase in levels. On the opposite side, increasing the levels leads to a large number of power semiconductors and associated driving circuitries. Hence, system cost and complexity are high. This affects system reliability and efficiency [10, 11]. Various multilevel inverter configurations were developed. Those configurations include neutral point clamped (NPC), cascaded H-bridge (CHB), flying capacitor (FC) and modular multilevel converters [12–15]. Those multilevel schemes can be configured to generate 3, 5, 7, or n-level output voltage [16]. NPC inverter was introduced by Akira Nabae and Akagi [17], as a three-level diode clamped form for motor drive. Stability and balancing of the dc-capacitors are a big concern of this topology, although it has only one dc-source. As the dc-capacitors are fed by the dc-source, capacitor voltage and current are controlled to keep the stability and balance of the two stacks [18]. Instead of clamping diode, Stillwell and Pilawa-Podgurski [19] used a FC to clamp the voltage of one capacitor voltage-level, which is a FC multilevel converter. FC multilevel inverter owns some distinct feature over the NPC counterpart, which is the phase redundancies. Such feature gives the FC flexibility in charging or discharging, and overcome voltage unbalance or faults.

Moreover, redundancy improves voltage stresses across the power switches and harmonic profile. Meanwhile FC multilevel inverter suffers from different drawbacks such as control complexity to manoeuvre voltage of all capacitors and poor switching efficiency [15, 18]. Another formation of multilevel inverter is the CHB multilevel converter, which is built by series-connected h-bridge inverters. Each bridge has its dc-source. The modularity of this formation gives it an obvious advantage over neutral point and FC configurations, it gives the inverter high flexibility in fault tolerance and low power level operation after cell failure [20]. Scalable technology or modular multilevel inverter is another power configuration of multilevel inverters. Where submodules with independent control systems are connected in cascade formation to generate any number of levels required. However, current circulation within the converter increases the overall conduction losses of the system and balancing the submodule capacitor is the main issue in controlling the modular multilevel topologies. This manuscript presents a new five-level boost inverter. Different five-level configurations are presented in the literature. Five-level formation presented in [21], can generate five-level output with six switches, two diodes and two capacitors. Although it has less number of switches, it requires a complex control algorithm for balancing the capacitors and diodes, deteriorating overall system efficiency.

The configuration presented in [22] is similar to the one presented in [21], as it is based on the switched capacitors cell, but designed to generate nine levels instead of five levels. Roy et al. [23] developed a cross-switched inverter based on switched-capacitor-converters, it utilises an optimum number of switches, however, its five-level version includes two capacitors, which would lead to more control complexity. Another distinct five-level topology is presented in [24]. However, it requires seven-switches, four-diodes, and two capacitors to generate the required five-level output. The new proposed configuration is a modification of the multilevel inverter configurations proposed in [25, 26]. Topologies presented in [25, 26] can generate nine-level but requires two dcsources with different voltage amplitude and in case of three-phase configuration, it requires six dc-sources. On the other hand, the proposed version in this study can generate a five-level output voltage with only one dc-source and one capacitor and in threephase configuration, still, one dc source is enough to implement thethree-phase output voltage. Another advantage of the proposed configuration over its counterpart in [25, 26] is its boosting ability, where the output voltage is higher than twice the input voltage. The proposed configuration generates five-level output voltage with amplitude double of the input voltage using only one dc-source, one-capacitor and eight power switches. Generated output voltage levels are (2Vdc, Vdc, $0, -\mathrm{Vdc}, -2\mathrm{Vdc}$). The general schematic representation of the proposed system is depicted in Fig. 1.

The system can be extended to the three-phase version by using three capacitors, and 24 power switches. In this study only single-phase configuration will be studied and investigated. The capacitor is connected in parallel in some states with the dc-source to be charged. Then it is reconnected to be in series with the dc-source to generate 2Vdc output voltage level. To drive the switches of the multilevel inverter, level-shift PWM (LS-PWM) is implemented in this study. The reference voltage is compared with four carriers to generate the required switching states. The study is organised as follows: Section 2 discusses operation modes of the developed multilevel boost-inverter. Section 3 discusses the modulation strategy while Section 4 considers calculation of the losses by the proposed configuration and Section 5 includes simulation and experimental results.

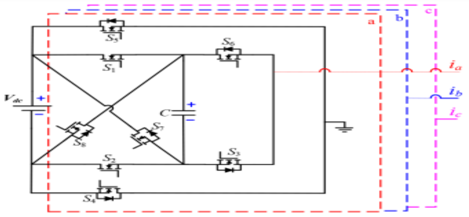


Fig. 1 *General Schematic representation of proposed five-level inverter*

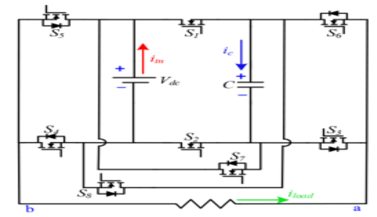
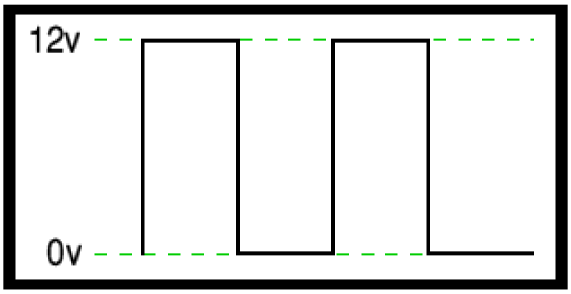


Fig. 2 *Single-phase configuration of the proposed five-level inverter*

II.PULSE WIDTH MODULATION

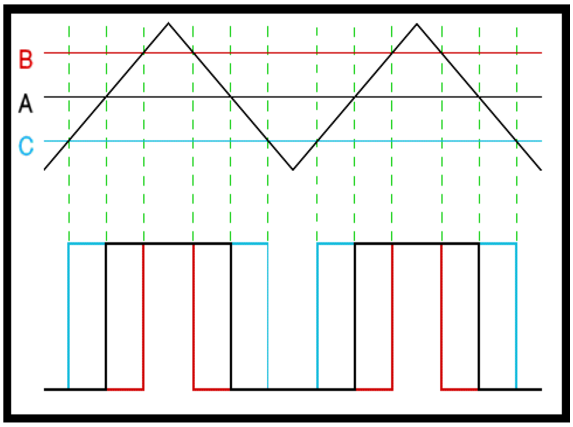
What is PWM?

Pulse Width Modulation (PWM) is the most effective means to achieve constant voltage battery charging by switching the solar system controller's power devices. When in PWM regulation, the current from the solar array tapers according to the battery's condition and recharging needs Consider a waveform such as this: it is a voltage switching between 0v and 12v. It is fairly obvious that, since the voltage is at 12v for exactly as long as it is at 0v, then a 'suitable device' connected to its output will see the average voltage and think it is being fed 6v - exactly half of 12v. So by varying the width of the positive pulse - we can vary the 'average' voltage.



Pulse Width modulator

So, how do we generate a PWM waveform? It's actually very easy, there are circuits available in the TEC site. First you generate a triangle waveform as shown in the diagram below. You compare this with a d.c voltage, which you adjust to control the ratio of on to off time that you require. When the triangle is above the 'demand' voltage, the output goes high. When the triangle is below the demand voltage, the



III. MULTI LEVEL INVERTER

An inverter is an electrical device that converts direct current (DC) to alternating current (AC) the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. The electrical inverter is a high power electronic oscillator. It is so named because early mechanical AC to DC converters were made to work in reverse, and thus were "inverted", to convert DC to AC.

3.1Cascaded H-Bridges inverter

A single phase structure of an m-level cascaded inverter is illustrated in Figure. Each separate DC source (SDCS) is connected to a single phase full bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the DC source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The AC outputs of each of the different full bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate DC sources. An example phase voltage waveform for an 11 level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure. The phase voltage

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$$

…(4.1)

For a stepped waveform such as the one depicted in Figure 4.2 with s steps, the Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_n [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)] \frac{\sin(n\omega t)}{n}, \quad where\ n = 1,3,5,7 \ldots$$

…(4.2)

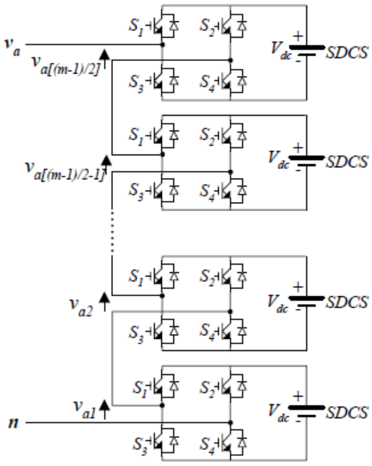


Fig.Single-phase structure of a multilevel cascaded H-bridges inverter

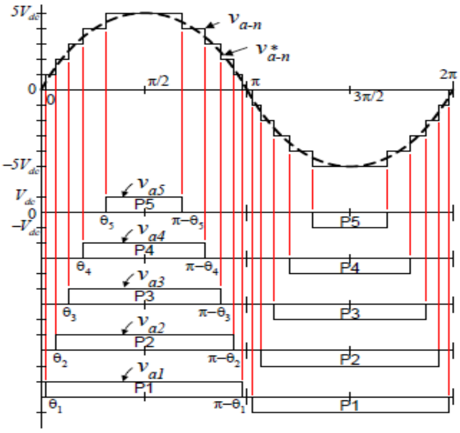


Fig. Output phase voltage waveform of an 11 level cascade inverter with 5 separate dc sources.

IV.PROPOSED SYTEM AND CONTROL DESIGN

Proposed five-level boost multilevel inverter

The proposed five-level boost multilevel inverter is depicted in Fig. 2. The proposed topology is a five-level multilevel inverter with boosting ability and the output voltage is double the input voltage. The developed topology has only eight switches, two of them are without anti-parallel diode. Although the proposed inverter has 28 possible switching states, only six valid switching states are implemented, as discussed in Table 1, to generate the five-level output voltage. All valid operation modes are depicted in Figs. 3 and 4. 2.1 Operation modes Mode 1, freewheeling occurs: the inverter generates output voltage equal to zero and capacitor C is charging from the dc-source (see Fig. 3a). During this analysis the capacitor is assumed to be charged when the capacitor voltage is zero, large inrush current is drawn. Indeed, most of the multilevel topologies with FCs would suffer from the same concern. In high power applications, a precharge device could be adopted, which allows capacitor voltage to build up gradually [27–32]. S1 , S2 , S3 and S4 are on, while the other switches are off. Capacitors C is charging from the dc source and has a voltage equal to the dc-source voltage. Capacitor C is charged from the input voltage and its steady-state value equals the input voltage. Output terminal a is connected to output terminal b. Mode 2: the inverter generates output voltage equals to the input voltage (see Fig. 3b), S1 , S2 , S3 and S5 are on, while the other switches are off. Capacitors C is charged from the dc source and has its voltage equal to the dc-source voltage. Output positive terminal b is connected to the positive terminal of the input source, while the terminal a is connected to the negative terminal of the dcsource. Mode 3: the inverter generates output voltage, which is equal to twice the input voltage (see Fig. 3c), switches S3 , S5 and S8 are on, while the other switches are off. Output positive terminal b is connected to the positive terminal of the dc-source, while terminal a is connected to the negative terminal of capacitor C. Mode 4, freewheeling occurs: the inverter generates output voltage equal to zero and capacitor C is charged from the dc-source (see Fig. 4a). S1 , S2 , S3 and S4 are on, while the other switches are off. C is charged from the dc source and has its voltage equal to the dc-source voltage. C is charged from the input voltage and it's steady-state value is equal to the input voltage. Output terminal b is connected to output terminal a. Mode 5: the inverter generates output voltage, which is equal to the input voltage (see Fig. 4b), S1 , S2 , S4 and S6 are on, while the other switches are off. C is charging from the dc source and has a voltage equal to the dc-source voltage. Output positive terminal b is connected to the negative terminal of the dc-source, while terminal a is connected to the positive terminal of the dc-source. Mode 6: the inverter generates output voltage equals to twice the input voltage (see Fig. 4c), S4 , S6 and S7 are on, while the other switches are off. Output positive terminal b is connected to the negative terminal of the dc-source, while terminal a is connected to the positive terminal of capacitor C. 2.2 Parameter design The selection of capacitance is important to ensure lower ripple amount on the capacitor voltage, large ripple in capacitor voltage may cause asymmetry in output voltage steps. According to the analysis in Figs. 3a, b and 4a, C is paralleled with the dc source and is charged. This leads to the following characteristic equations:

$$\{v_c = v_{dc} \Leftrightarrow i_c = i_{in} \tag{1}$$

In mode displayed in Fig. 4a, C is still being charged. However, its current equation is different from the previously mentioned equation and it could be marked as

$$\{v_c = v_{dc} \Leftrightarrow i_c = i_{in} - i_{load} \tag{2}$$

C is discharging in modes described in Figs. 3c and 4b, and capacitor characteristics equation during these modes is

$$\{v_c = v_0 - v_{dc} \Leftrightarrow i_c = i_{in} \tag{3}$$

A graph of capacitor voltage is depicted in Fig. 5. From the graph and (1–3), C could be selected as follows:

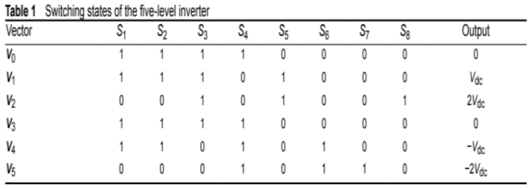


Table 1 Switching states of the five-level inverter

Vector	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output
V_0	1	1	1	1	0	0	0	0	0
V_1	1	1	1	0	1	0	0	0	V_{dc}
V_2	0	0	1	0	1	0	0	1	$2V_{dc}$
V_3	1	1	1	1	0	0	0	0	0
V_4	1	1	0	1	0	1	0	0	$-V_{dc}$
V_5	0	0	0	1	0	1	1	0	$-2V_{dc}$

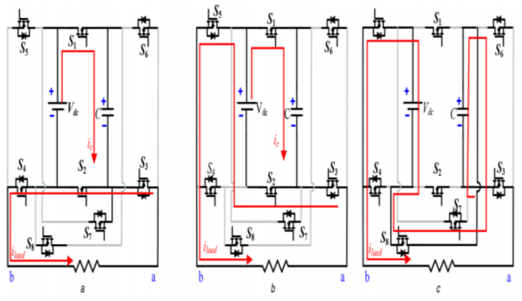


Fig. 3 *Operation modes*
(a) Mode I, (b) Mode II, (c) Mode III

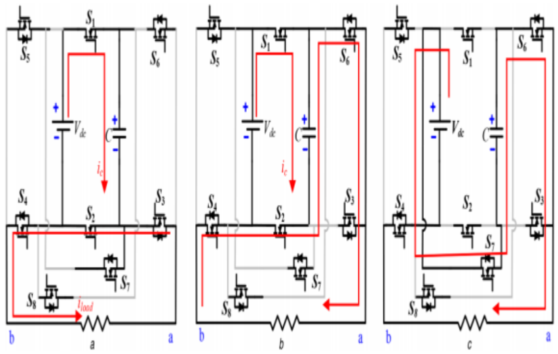
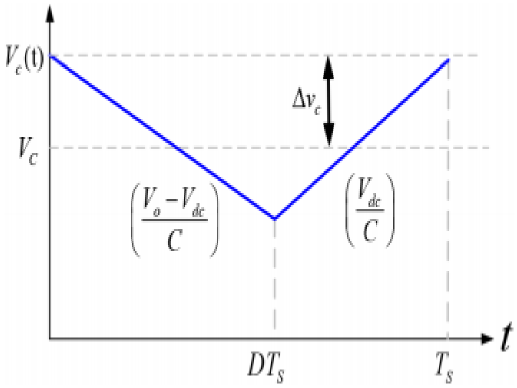


Fig. 4 *Operation modes*
(a) Mode IV, (b) Mode V, (c) Mode VI

$$C = \left(\frac{v_o - v_{dc}}{2\Delta v_c}\right) DT_s \qquad (4)$$

As indicated, C depends on the input voltage vdc, the output voltage vo , sampling time Ts , accepted amount of ripple in capacitor voltage Δvc , and the duty ratio D. The voltage and current stresses of components are summarised in Table 2. All the switching devices have similar current stresses. However, different voltage stresses are observed. S7 and S8 exhibit the highest voltage stress, which equals the output voltage. Other switches are having voltage stress equal to the input voltage. It should be noted that due to the circuit asymmetry, the voltage stresses of S7 and S8 are higher than that of the other switches. Thus, special attention needs to be paid in component selection.

Level shift pulse width modulation



PWM is widely used to drive the switches of power converters (dc or ac converters) at a given switching frequency. Pulses pattern generated by the PWM block is implemented in a way to give a higher modulation index and less harmonic profile of the output waveform. Moreover, modulation schemes can be designed to reduce switching losses, current ripple, and balance capacitor voltage. In the two-level converter, a single triangular carrier is compared with the modulation signal to develop the switching pattern of the switches.

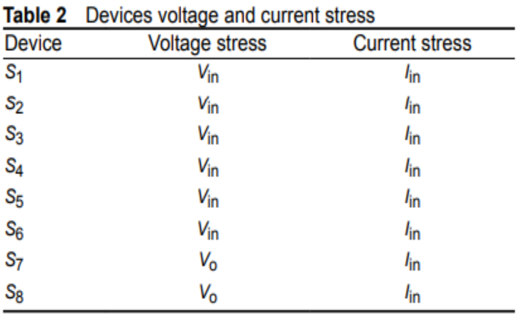


Table 2 Devices voltage and current stress

Device	Voltage stress	Current stress
S_1	V_{in}	I_{in}
S_2	V_{in}	I_{in}
S_3	V_{in}	I_{in}
S_4	V_{in}	I_{in}
S_5	V_{in}	I_{in}
S_6	V_{in}	I_{in}
S_7	V_o	I_{in}
S_8	V_o	I_{in}

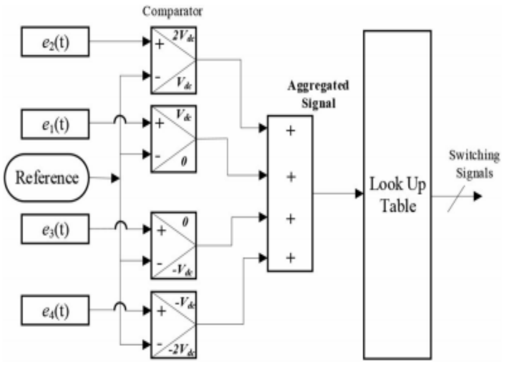


Fig. 6 *Switching signal generation schematic diagram*

V.SIMULATION RESULTS

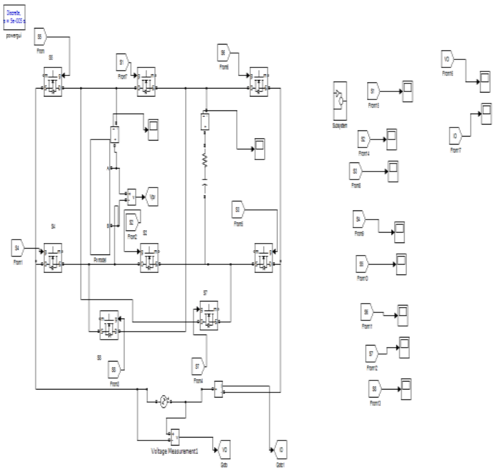


Fig .simulink model

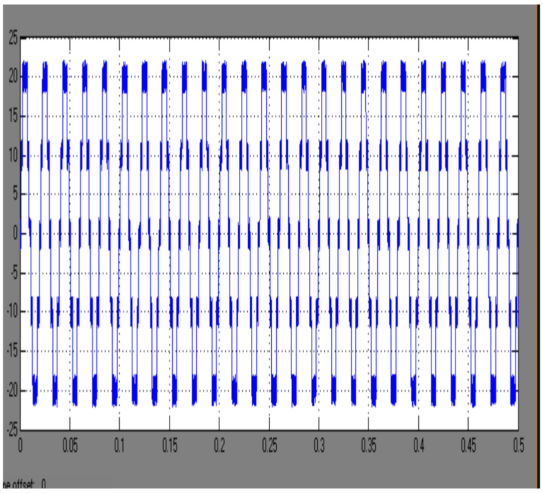


Fig grid currents

Each switching device incurs two types of losses; conduction losses when the device is conducting and switching losses when the device is switching (change state from off to on and vice versa). In each switching state, of the eight possible states, at least three switches are turned on or switched to be on. This leads to two types of losses, conduction losses and switching losses. In the upcoming sections, analytical calculation for the switching and conduction losses is discussed. 4.1 Conduction losses The proposed topology has eight switches, two of its power switches and unidirectional conducting and blocking while the remaining six switches are unidirectional blocking and bidirectional conducting, the instantaneous conduction losses of the power switch and its body diode can be given as [14, 24]

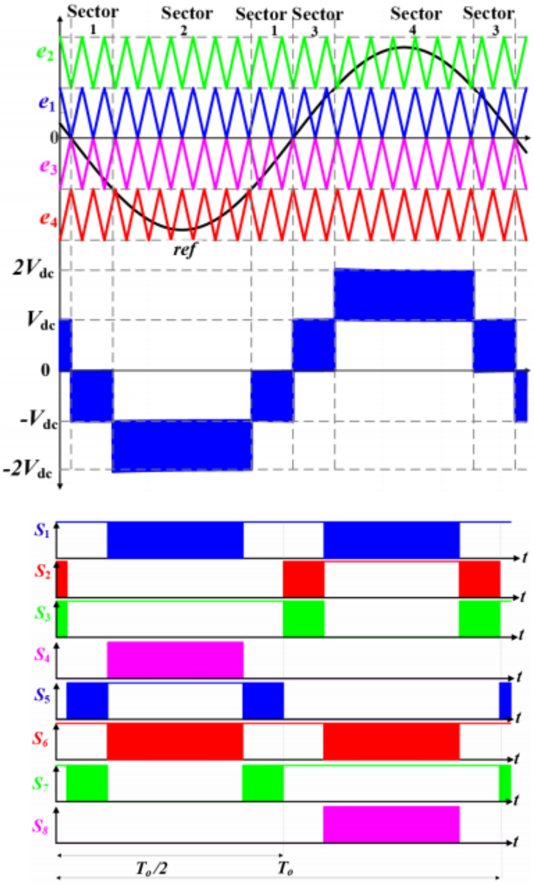


Fig. 8 *Driving signals of the five-level inverter*

$$\rho_{c,T}(t) = \left[V_T + R_T i^{\alpha}(t)\right] i(t) \tag{5}$$

$$\rho_{c,D}(t) = \left[V_D + R_D i(t)\right] i(t) \tag{6}$$

The average conduction losses are expressed as

$$\rho_{c,avg} = \frac{1}{\Pi}\int_0^{\Pi} \left[\begin{array}{c} \{N_T(t)V_T + N_D(t)V_D\} i_L(t) \\ + \{N_T(t)R_T i_L^{\alpha+1}(t)\} + \{N_D(t) i_L^2(t)\} \end{array}\right] d(\omega t) \tag{7}$$

where ρc,T(t), ρc,D(t), VT, VD, RT, RD, α, ND, NT and ρc, avg(t) denote the instantaneous conduction losses of the transistor, the instantaneous conduction losses of the diode, transistor on-state voltage drop, diode instantaneous voltage drop, transistor equivalent on-resistance, diode equivalent on-state resistance, constant given by transistor characteristics, number of conducting diodes, number of conducting transistor and average conduction losses, respectively.

Switching losses

Switching losses of each switching device can be estimated using a linear approximation of voltage and current during the switching period, [14, 24]. Turn-on energy losses can be calculated as

$$E_{\mathrm{on},j} = \int_0^{t_{\mathrm{on}}} \left\{ \left[V_{\mathrm{o},j} \frac{t}{t_{\mathrm{on}}} \right] \left[-\frac{I}{t_{\mathrm{on}}}(t - t_{\mathrm{on}}) \right] \right\} \mathrm{d}t = \frac{1}{6} V_{\mathrm{o},j} I t_{\mathrm{on}} \qquad (8)$$

Similarly, energy losses of the *j*th switch during turning off are calculated as

$$E_{\mathrm{off},j} = \int_0^{t_{\mathrm{off}}} \left\{ \left[V_{\mathrm{o},j} * \frac{t}{t_{\mathrm{off}}} \right] \left[-\frac{I}{t_{\mathrm{off}}}(t - t_{\mathrm{off}}) \right] \right\} \mathrm{d}t = \frac{1}{6} V_{\mathrm{o},j} I t_{\mathrm{off}} \qquad (9)$$

where Eon, j , ton, I, Vo , j Eoff, j and toff denote to turn-on loss of the jth switch, turn-on time, current through the switch after turning on, voltage of the jth switch during turning off, turn-off loss of the jth switch, and turn-off time, respectively. Total switching power losses can be calculated as:

$$\rho_S = \sum_{j=1}^{2n+2} \left[\frac{1}{6} V_{\mathrm{o},j} * I(t_{\mathrm{on}} + t_{\mathrm{off}}) f_j \right] \qquad (10)$$

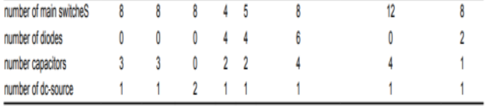
A graph of the inverter efficiency is depicted in Fig. 9. The optimum operating power range for the proposed inverter is between 350 and 650 W. However, in all power range up to 800 W, its efficiency is >95%.

VI.CONCLUSION

A five-level boost multilevel inverter was presented in this study. The single-phase version's designed configuration, made up of just one DC capacitor and eight switches. With an amplitude greater than twice the input voltage, it can produce a five-level output. In this design, the balancing problem is not present because only one capacitor is used.

The suggested inverter is a competitive alternative for PV system applications because of its boosting capability. After being charged by the DC source, the DC capacitor is rearranged so that it is in series with the DC source. Higher output voltage can therefore be achieved. LS-PWM is used to drive the inverter's switches. The purpose of switching states is to guarantee that the capacitor has enough time to charge and that there isn't a significant voltage ripple.

Table 3 Component requirements for single-phase five-level multilevel inverter



Topology	NPC [34]	FC [19]	CHB [35]	[10]	[36]	Diode clamped [37]	Capacitor clamped [38]	This work
number of main switcheS	8	8	8	4	5	8	12	8
number of diodes	0	0	0	4	4	6	0	2
number capacitors	3	3	0	2	2	4	4	1
number of dc-source	1	1	2	1	1	1	1	1

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