Journal of **N**onlinear **A**nalysis and **O**ptimization
Vol. 11, Issue. 2 : 2020
ISSN : **1906-9685**

EMBEDDED TRANSITION INVERSION CODING WITH LOW SWITCHING ACTIVITY FOR SERIAL LINKS

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ABSTRACT:
The embedded transition inversion (ETI) is proposed to reduce bit transitions in serializing parallel buses. Implies power can be reduced further. This project proposes an embedded transition inversion (ETI) coding scheme that uses the phase difference between the clock and data in the transmitted serial data to tackle the problem of the extra indication bit. The technique is implemented in an optimized fashion using pipelining so that it can be used in practical systems with only a slight compromise in performance. This is achieved by calculating the decision as the data is being loaded on to the buffer and doing the encoding on the fly. This is one aspect which is lacking in most existing algorithms as they are not amenable to low delay implementation.

1. INTRODUCTION

Advanced silicon technology offers the possibility of integrating hundreds of millions of transistors into a single chip, which makes system-on-chip (SoC) design possible. With the continuous scaling of silicon technology, area and power dissipation of interconnects are one of the main bottlenecks for both on-chip and off-chip buses. Multiplexing parallel buses into a serial link enables an improvement in terms of reducing interconnect area, coupling capacitance, and crosstalk, but it may increase the overall switching activity factor (AF) and energy dissipation. Therefore, an efficient coding method that reduces the switching AF is important issues in serial interconnect design. The embedded transition inversion (ETI) coding scheme reduce the switching activity factor and solve the extra bit indication of TIC coding scheme by embedding the inversion information in the phase difference between the clock and the encoded data.

When there is an inversion in the data word, a phase difference is generated between the clock and data. Otherwise, the data word remains unchanged and there is no phase difference between the clock and the data. Need of phase difference is decided by the decision bit. The decision bit is decided by the no. of transitions when the no. of transitions are more than half of the word length, every even bit of the data word will be inverted and then decision bit sets to high. This operation is performed at transmitted section.

The receiver side adopts a phase detector (PD) to detect whether the received data word has been encoded or not. Statistical analysis and experimental results show that the proposed coding scheme has low transitions for different

kinds of data patterns. Low power design, in a system perspective, happens at all levels of the digital electronic system stack. It is being done from the lowermost device level design to the topmost software design. And there are the intermediate levels where a lot of effort is being expended to make systems run at low power. This scheme eliminates the need of sending an extra bit by embedding the inversion information in the phase difference between the clock and the encoded data. When there is an inversion in the data word, a phase difference is generated between the clock and data. Otherwise, the data word remains unchanged and there is no phase difference between the clock and the data. The receiver side adopts a phase detector (PD) to detect whether the received data word has been encoded or not. A significant improvement in the interconnect energy dissipation is achieved by applying different word lengths by degree of multiplexing. However, the power reduction decreases when the degree of multiplexing increases. The Modified Embedded Transition Inversion (ETI) Coding scheme reduces the power consumption using sequential element. Advanced silicon technology offers the possibility of integrating hundreds of millions of transistors into a single chip, which makes system-on-chip (SoC) design possible. With the continuous scaling of silicon technology, area and power dissipation of interconnects are one of the main bottlenecks for both on-chip and off-chip buses. Multiplexing parallel buses into a serial link enables an improvement in terms of reducing interconnect area, coupling capacitance, and crosstalk [1], but it may increase the overall switching activity factor (AF) and energy dissipation. Therefore, an efficient coding method that reduces the switching AF is an important issue in serial interconnect design. Many studies attempt to reduce the AF of parallel buses. For example, Stan and Burleson [2] introduced a bus-invert method that transmits the original or inverted pattern to minimize the switching activity. Researchers have proposed many techniques to improve the bus-invert coding method, such as the partial bus-invert coding [3] and weight-based businvert coding methods [4]. The schemes mentioned above use an extra channel to send the inversion indication signal. Kuo et al. [5] proposed the serial coding technique to solve the extra channel problem. They append extra information bits to the back of the original data word. Although this approach resolves the area overhead problem, it increases data latency. Three level differential encoding is proposed for parallel bus [6] to enable multiple drivers at the transmitter and to recycle the same current and reduce power consumption [6]. Joint crosstalk avoidance code and error correction code are proposed to reduce the power in parallel bus [7]. Huang et al. [8] further proposed combining serializing bus with the joint crosstalk avoidance code and error correction code to reduce the power. Serialized low-energy transmission (SILENT) [1] is a coding method used in reducing the switching activity for serial links. This approach encodes every single bit in the parallel bus using the XOR gate, and multiplexes the encoded parallel buses into a serial link. The XOR operation sets an adjacent bit with the same value to zero. The greater the correlation is, the more zeros the encoder produces. This method is designed for data with strong correlation. Bharghava et al. [9] proposed the transition inversion coding (TIC) technique to reduce switching activity for random data and to detect errors. Their technique counts the transitions in the data word, and inverts the transition states if the number of transitions in a data word is more than half of the word length. The scheme sets the current bit in the serial stream to be the same as the previous encoded bit when there is a transition. Otherwise, it is set to the inversion of the previous encoded bit. A transition indication bit is added in every data

word. This extra bit not only increases the number of transmitted bits, but also increases the transitions and latency. Lee et al. [10]– [12] used serial links as communication channels on an on-chip network architecture for SoC. The serial links reduce the area of communication channels by 57% compared with a nonserialized approach [10]. This approach also reduces the switch activity because the coupling capacitance of the interconnect wires decreases [10]–[12]. Forward error correction (FEC) code is used to reduce the serial link power by trading off the FEC coding gain with specifications on transmit swing, analog-to-digital converter precision, jitter tolerance, receive amplification, and by enabling higher signal constellations [13]. By combining the single and differential signals and 8B/10B coding, a high speed phase tracking clock recovery is developed for serial link to reduce the power [14]. To utilize the relation between data in a link, the encoder reorders or shuffles the M bits in the parallel bus such that the encoded data are less correlated or silent [15]. Then the encoded data are serialized with one control bit. The silent coding with shuffling can reduce the power dissipation compared to the silent coding

2. LITERATURE SURVEY

Parallel buses multiplexed into a serial link enables an improvement in terms of reducing interconnect area, coupling capacitance, and crosstalk, but it increases the overall switching activity factor (AF) and energy dissipation .Therefore, an efficient coding method needed to reduce the switching AF is an important issue in serial interconnect design. Many studies attempt to reduce the AF of parallel buses. Stan and Burleson introduced a bus-invert method that transmits the original or inverted pattern to minimize the switching activity. Researchers have proposed many techniques to improve the bus-invert coding method, such as the partial bus-invert coding and weight-based bus invert coding methods. The schemes mentioned above use an extra channel to send the inversion indication signal.

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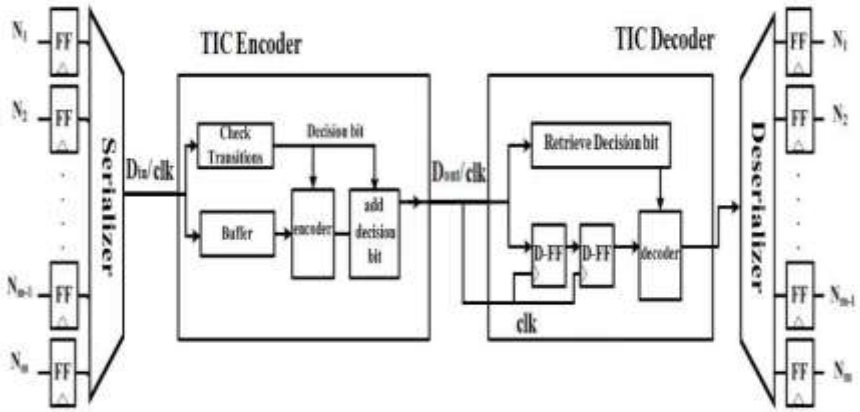
number of transmitted bits, but also increases the transitions and latency. Serial links as communication channels on on-chip network architecture for SoC. The serial links reduce the area of communication channels by 57% compared with a non serialized approach. This approach also reduces the switch activity because the coupling capacitance of the interconnect wires. The embedded transition inversion (ETI) coding scheme is proposed to solve the extra bit indication. This scheme eliminates the need of sending an extra bit by embedding the inversion information in the phase difference between the clock and the encoded data. When there is an inversion in the data word, a phase difference is generated between the clock and data. Otherwise, the data word remains unchanged and there is no phase difference between the clock and the data. The improvement of transition reduction is 19% compared with that of the TIC. The receiver side adopts a phase detector (PD) to detect whether the received data word has been encoded or not.

3. EXISTING SYSTEM

TRANSITION INVERSION CODING



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The embedded transition inversion coding (ETI) coding scheme to solve the TIC coding scheme issue of the extra indication bit [7]. The ETI scheme eliminates the need of sending an extra bit by embedding the inversion information in the phase difference between the clock and the encoded data. When there is an inversion in the data word, a phase difference is generated between the clock and data. Otherwise, the data word remains unchanged and there is no phase difference between the clock and the data. The improvement of transition reduction is 19% compared with that of the TIC. The receiver side adopts a phase detector (PD) to detect whether the received data word has been encoded or not.

DRAWBACKS:

1. more area occupancy
2. More propagation delay
3. Un necessary glitters are produced
4. Low Throughput

4. PROPOSED ARCHITECTURE:

ETI ARCHITECTURE:

The TIC is one of the methods developed for random data [9]. This method adds a transition indication bit to every data word to indicate if there is an inversion or not. This inversion coding is performed on every bit of two consecutive bits in the serial stream. The extra indication bit increases the switching activity .The ETI coding scheme that operates on a two-bit basis and removes all the transition indication bits. The architecture of ETI coding scheme shown in below Fig.3.3.

The ETI architecture mainly contains the four sections

i) Serialization
ii) ETI encoder
iii) ETI decoder
iv) Deserialization

Each serial link has m input bit streams that are multiplexed by a serializer, followed by the ETI encoding. The encoded stream is transmitted through the serial link and followed by the ETI decoding and a deserializer.

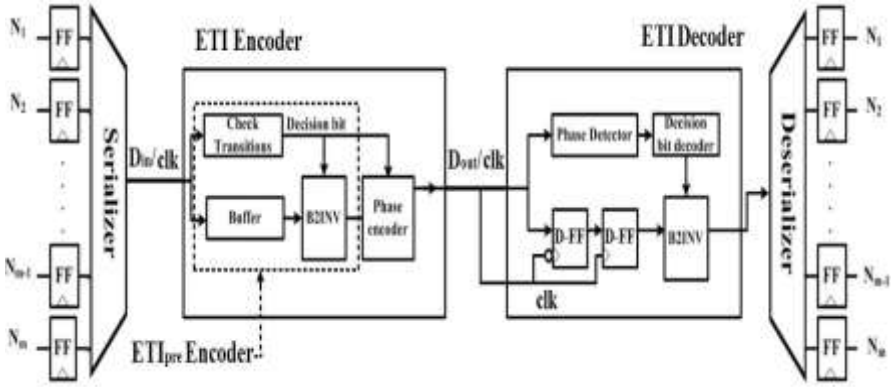


Fig:1. ETI architecture

Serialization:

Serial communication has many advantages over multi bit parallel communication in respects of signal skew, crosstalk, area cost, and wiring congestion. We propose multiplexing the data of bus lines onto one line (a serial link).

This converts the parallel –line bus into serial links, which reduces the number of physical bus lines, for the same bus area, this reduction in the number of bus lines leads to a larger interconnect width and pitch (area). The larger line pitch reduces the coupling capacitance, while the wider interconnects reduce the resistivity, leading to a significant improvement in the interconnect energy dissipation and delay. The reduction in delay can be transformed into a further energy reduction by reducing the number and size of required repeaters. By carefully selecting the number of serial links in the bus, a significant improvement in the overall energy dissipation can be achieved. This improvement increases as technology scales.

Serialization with n/m ETI serial links with n input bit streams under degree of multiplexing m. Fig3.4. Each serial link has m input bit streams that are multiplexed by a

serializer, followed by the ETI encoding The encoded stream is transmitted through the serial link and followed by the ETI decoding and a deserializer. The example for serializer is shown in Fig. 3.5.

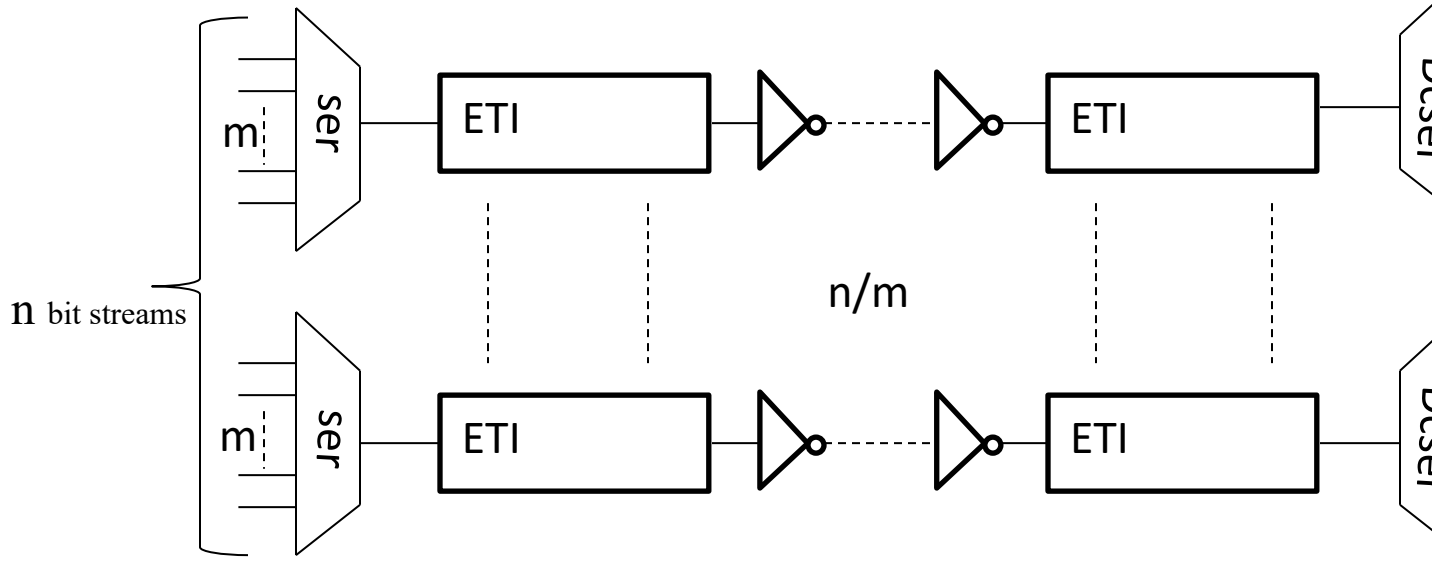
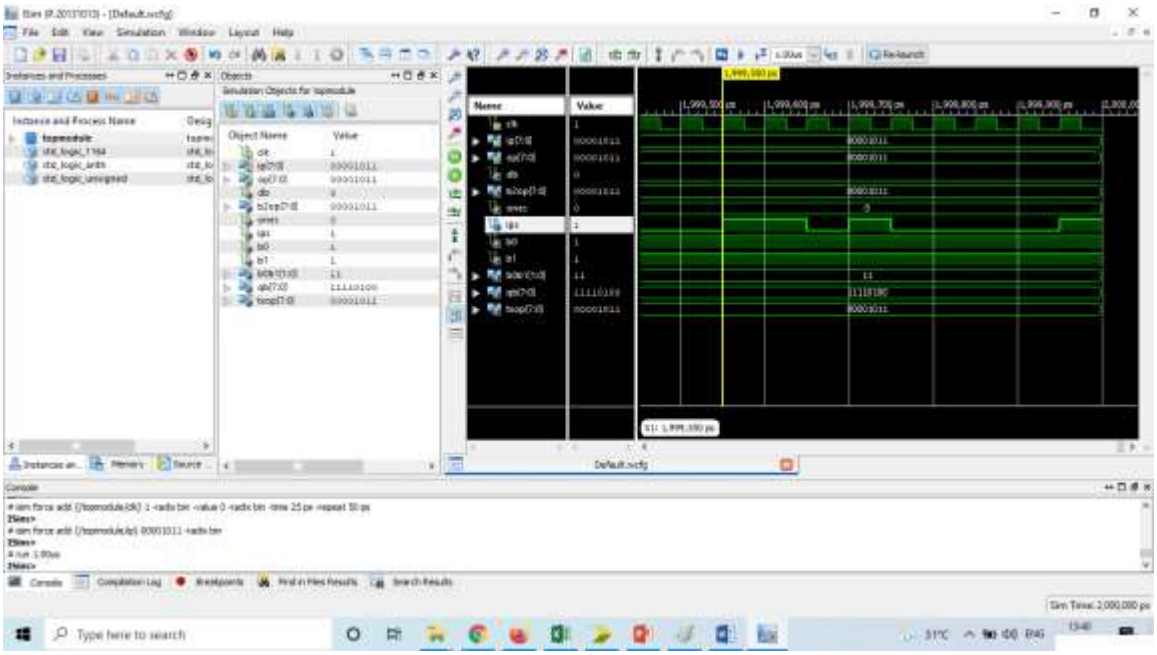
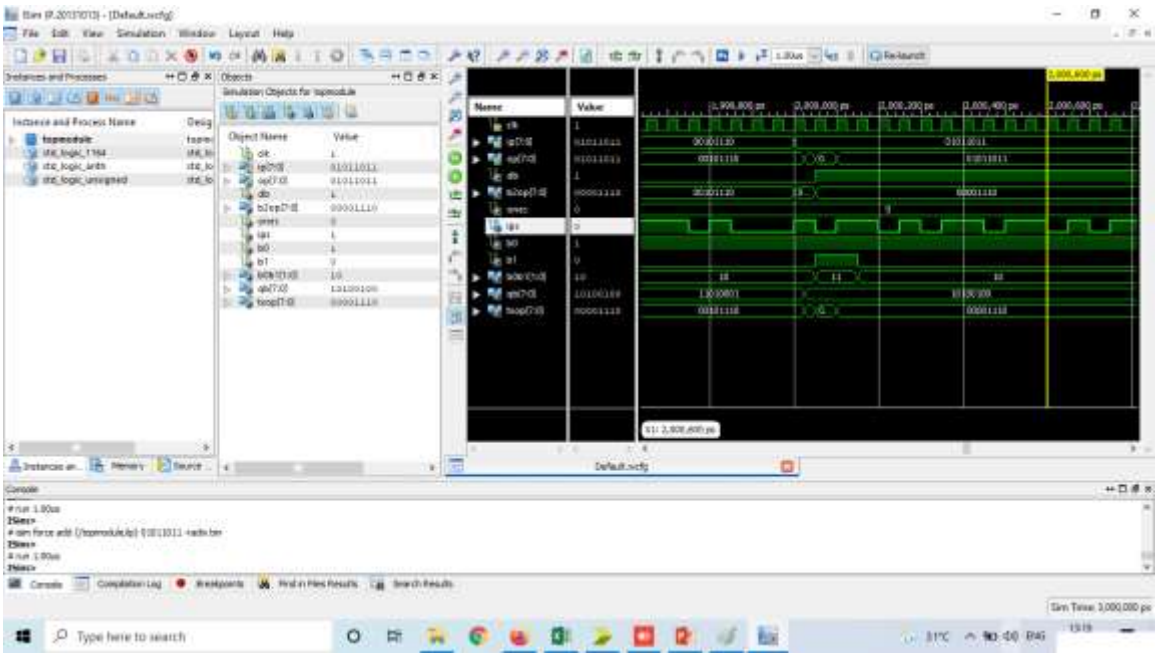


Fig : 2. n/m serial links with n input bit streams under the degree of multiplexing m

5. RESULTS:





ADVANTAGES

i. Low latency

ii. Low hardware over area head.

iii. Less complexity

APPLICATIONS

i. Communications: Zigbee, Bluetooth

ii. Biomedical: CRO with ECG

iv. Computers: System with keypad, mouse

6. CONCLUSION:

The ETI scheme is reduces the extra bit used in the TIC scheme and reduces the crosstalk, energy dissipation. ETI scheme uses the phase difference between the data and clock to indicate the bit inversion. In this thesis, the proposed ETI scheme is reduces the time, crosstalk and power compare with the existing ETI scheme. This enhanced technique is more useful in multipurpose applications due to the reason that it has low latency, power consumption factors.

FUTURE SCOPE:

The proposed hardware can be emulated on an Application Specific Integrated Circuit (ASIC) which can be used in the encoding algorithms where smaller area is necessary. Utilizing the parallelism and pipelining feature of the FPGA various Data compression algorithms (Huffman, Lempel-Ziv, Arithmetic and Shannon-Fano) can be delineated.

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